

### **REMARKS**

Claims 1, 2 and 4-33 were examined and reported in the Office Action. Claims 1 and 28-33 are rejected. Claims 2-27 are allowed. Claims 1, 2, 4-16, 18-22, 24-28 and 31 are amended. Claims 1, 2 and 4-33 remain.

Applicant requests reconsideration of the application in view of the following remarks.

#### **I. 35 U.S.C. §102(b)**

It is asserted in the Office Action that claims 1 and 28-33 are rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 6,009,011 issued to Yamauchi ("Yamauchi"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

[a] method for operating a non-volatile dynamic random access memory (NVD RAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising: preparing a power-on mode for performing a DRAM operation by controlling a threshold voltage of the transistor; and preparing a power-off mode for storing a data included in the capacitor into the floating gate.

Applicant's amended claim 28 contains the limitations of

[a] non-volatile dynamic random access memory (NVD RAM) device including a plurality of memory cells in a matrix, each memory cell comprising: a capacitor for storing a data; and a transistor for transmitting the data stored in the capacitor to a bit line, wherein the transistor includes a drain, a source, and a gate having a control gate and a floating gate for storing the data when a power is off and a threshold voltage of the transistor is controlled when the power is on, wherein one terminal of the capacitor is coupled to the drain of the transistor and the other terminal of the capacitor is supplied with a controllable voltage determined according to an operation mode.

And Applicant's amended claim 31 contains the limitations of

[a] non-volatile dynamic random access memory (NVD RAM) including a plurality of memory cells in a matrix, wherein each memory cell includes: a control gate layer coupled to a word line; a capacitor for storing data; and a floating transistor for transmitting the stored data in the capacitor to a bit line and storing the data therein in response to an operation mode, wherein a threshold voltage of the floating transistor is controlled when the power is on, wherein one terminal of the capacitor is coupled to a drain of the floating transistor and the other terminal of the capacitor is supplied with a controllable voltage determined according to the operation mode.

Yamauchi discloses a non-volatile memory. Yamauchi, however, does not teach, disclose or suggest the limitations contained in Applicant's: amended claim 1 of "preparing a power-on mode for performing a DRAM operation by controlling a threshold voltage of the transistor," amended claim 28 of "a gate having a control gate and a floating gate for storing the data when a power is off and a threshold voltage of the transistor is controlled when the power is on," or amended claim 31 of "a threshold voltage of the floating transistor is controlled when the power is on."

Therefore, since Yamauchi does not disclose, teach or suggest all of Applicant's amended claims 1, 28 and 31 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Yamauchi. Thus, Applicant's amended claims 1, 28 and 31 are not anticipated by Yamauchi. Additionally, the claims that directly or indirectly depend on claims 28 and 31, namely claims 29-30, and 32-33, respectively, are also not anticipated by Yamauchi for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1 and 28-33 are respectfully requested.

## **II. Allowable Subject Matter**

Applicant notes with appreciation the Examiner's assertion that claims 2-27 are allowed.

Applicant respectfully asserts that claims 1, 2 and 4-33, as it now stands, are allowable for the reasons given above.

**CONCLUSION**

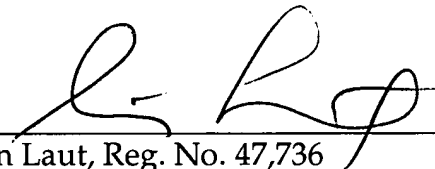
In view of the foregoing, it is submitted that claims 1, 2 and 4-33 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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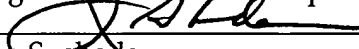
Dated: September 19, 2005

By:   
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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on September 19, 2005.

  
Jean Svoboda